ELEC 353 Research Project: Applications of Differential Amplifiers

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I. Differential Amplifiers in the Automotive Industry

The first application of differential amplifiers that will be examined in this report is their usage in the automotive industry. Electronic control and communication continues to be of high importance in automotive operation. However, there is one major issue with implementing digital communications between electronics in an automobile, which is noise and its effect on signal integrity. Voltage transients and other noise originate from the high-power electrical devices on the vehicle, namely the spark plugs and broader engine ignition system [1]. Each time a spark plug creates a spark to ignite fuel there is a large spike in current draw, leading to an electromagnetic emission that creates a voltage transient in other wires of the car's electrical system. For this reason, differential amplifiers are needed to facilitate digital communication in high noise environments. Differential amplifiers have the useful property of rejecting common mode voltages in accordance with their CMRR value. Thus, if a data signal is transmitted differentially, any voltage transient will appear equally on both lines of the differential pair and be attenuated significantly by the amplifier's CMRR, significantly improving reliability of data transmission and noise tolerance. The widespread requirement for reliable communication in high noise environments led directly to the development of the Controller Area Network (CAN) bus.

A. CAN Introduction

CAN is serial communication protocol that makes use of a differential pair to transmit data between multiple nodes on the bus [2]. The standard defines both physical and link layers, however, the focus will be placed on the implementation of differential amplifiers in the physical layer of the protocol specification.

B. CAN Implementation

The physical implementation of CAN bus consists of communication nodes all connected to the same differential pair signals, `CANH` and `CANL`. Each node includes the circuitry needed to send and receive messages on the bus. The differential impedance of the bus is fixed using bus termination resistors of approximately $120\,\Omega$ [3]. An example topology of the bus is given in Figure 1.

Each CAN node consists of 3 devices: a processor, controller and transceiver. The transceiver is of primary concern, as it is the component that performs the bi-directional conversion of differential and single ended signals so that the controller and processor can interact with the bus [3]. The transceiver performs this using differential amplifiers. A common CAN node structure is given in Figure 2.

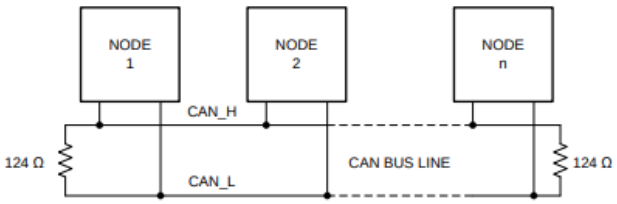


Figure 1. Example CAN bus topology for a bus with n nodes. [3]

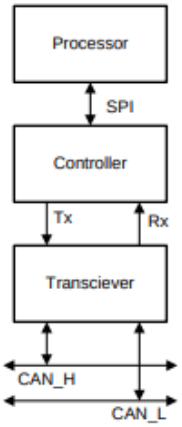
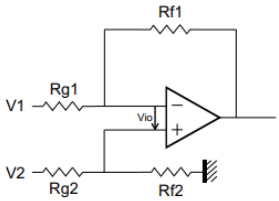


Figure 2. Common structure for a CAN node, consisting of a transceiver which is connected to a controller, which is in turn connected to a processor via a SPI bus [3].

C. Transceiver Circuitry

The CAN transceiver must perform two tasks: conversion of the differential signal on the CAN bus to a single-ended `Rx` signal to be interpreted by the controller, and conversion of the single-ended `Tx` signal from the controller to a differential signal which it drives on the bus. Conversion from differential to single-ended output is implemented using an operational amplifier, whose inputs are connected to the differential signals of the bus. Feedback resistors are added in order to calibrate the output voltage range to the desired value [4]. Figure 3 shows a common implementation and the resulting formula for output voltage.

For converting a single-ended input to a differential output in order to transmit data onto the bus, a traditional differential amplifier is used with the inverting input grounded. The two outputs of the amplifier serve as the differential output signal. An example implementation from Analog Devices is given in Figure 4.



$$V_{out} = V_2 \frac{R_{f2}\left(1+\frac{R_{f1}}{R_{g1}}\right)}{R_{g2}\left(1+\frac{R_{f2}}{R_{g2}}\right)} - V_1 \frac{R_{f1}}{R_{g1}}$$

Figure 3. Conversion circuit from differential to single ended output [4].

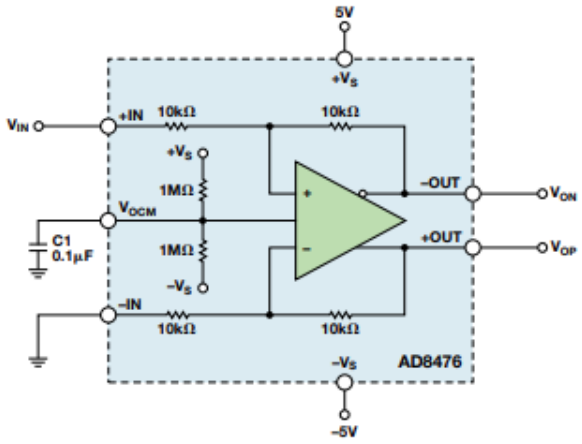


Figure 4. Conversion circuit from single ended to differential output [5].

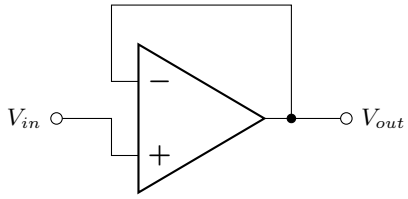


Figure 5. An operational amplifier configured as a negative-feedback unity-gain buffer.

D. Issues

The receive and transmit circuits implemented above present the major drawback of the usage of CAN and other communications standards which are based on the differential pair, which is solution complexity and cost. Adding a CAN controller and transceiver to each node on the bus will inevitably increase implementation cost, and a higher part count can lead to lower reliability. Moreover, there is additional design overhead resulting from the addition of CAN controllers and transceivers and associated discrete components, all of which must be properly connected in the schematic. Overall, the benefits far outweigh the drawbacks, specifically the ability to move data quickly between devices in a high noise environment, satisfying the requirements of the automotive application.

II. Differential Amplifiers in Digital to Analog Conversion

A. Overview

Operational amplifiers are used in a variety of configurations to buffer the output port of digital-to-analog converters (DACs). The effect of this is to lower the output impedance, allowing a load to draw a much larger current while maintaining high signal fidelity. Depending on the op-amp configuration, other potentially desirable effects, such as amplification or voltage bias/offset, may be introduced as well.

One such configuration is the negative-feedback unity-gain buffer, shown in Figure 5. This is one of the more common configurations, used in many DAC ICs, such as the TIDA-01402 from Texas Instruments [6].

This is not the only possible configuration. Another design, shown in Figure 6, was devised to maintain reasonable signal fidelity at extremely high sample output rates (up to 20 GHz). This uses a custom, specialized op-amp circuit which combines common-drain and common-source NMOS configurations to achieve high gain and low

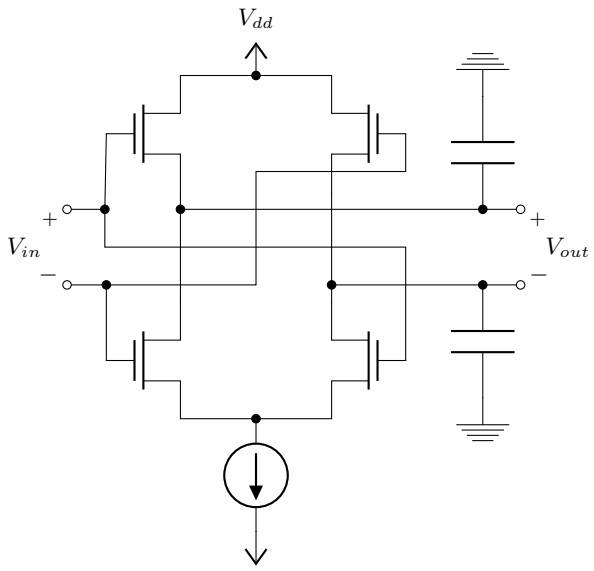


Figure 6. Specialized broadband differential buffer design devised by Singh and Gupta [7].

output impedance, while providing extremely high input impedance. Note that it is designed to be used with a DAC which provides a differential output signal [7], and it itself drives a differential transmission line.

B. Issues

Using op-amp buffers on DACs is not without cost. The buffer will inevitably, as a result of the finite gate capacitance at its input terminals, act as a low-pass filter which could attenuate and distort the signal, albeit only at very high frequencies; the buffer design should thus incorporate the desired frequency band. In addition, the op-amp will of course add to the die size and manufacturing cost of the chip, though the significance of this effect depends on the exact application.

C. Buffer Necessity

The primary reason for incorporating a buffer into a DAC application is to reduce an otherwise large output impedance to be negligibly small. For example, the STM32F407 microcontroller includes DAC outputs, which can optionally (software-controlled) be buffered [8]. Without the buffer connected, the DAC pin has an output impedance of up to $15\,\mathrm{k}\Omega$. If this were to be connected to a resistive load such as a speaker—which would typically have an impedance under $10\,\Omega$—the resulting signal attenuation (on the order of $64\,\mathrm{dB}$ in this case) would render the device effectively unusable. Similarly, if this were to be connected to a capacative load (such as a transmission line) and drive out an AC signal, the resulting RC circuit would create a low-pass filter with a cutoff frequency low enough to likely cause issues.

The fairly simple inverting buffer provided in the STM32F407, when enabled, eliminates these issues, using an op-amp feedback loop design [8]. In fact, when the buffer is enabled, the primary concern in determining if a load can be driven by the DAC is the current draw limit of the pin. This is the reason why the internal buffer can be disabled: to permit an external buffer with characteristics more aligned to the application at hand.

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